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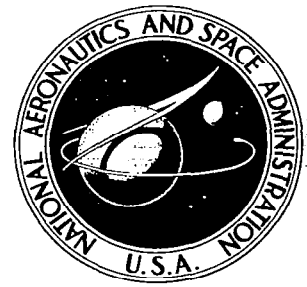

FEASIBILITY BREADBOARD OF AN ALL-MAGNETIC PCM TELEMETRY SYSTEM

by C. H. Heckler, Jr., and J. A. Baer

Prepared by
STANFORD RESEARCH INSTITUTE
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ABSTRACT

A feasibility breadboard of an all-magnetic PCM telemetry system has been constructed in this second phase. The design is a modification of the logic design of the twelve-channel PCM telemetry system made in the first phase. The breadboard uses fewer magnetic cores and transistors than estimated for the original design. The system is completely digital, departing from the conventional design, which requires the amplification of analog signals. The novel magnetic circuits found in the first phase have received limited testing and are used in this breadboard. The estimated power consumption is less than two and one-half watts.

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I INTRODUCTION

The use of all-magnetic circuit techniques to improve system reliability is an interesting potential method of increasing reliability of spaceborne digital systems. All-magnetic circuits use only wire and square-loop magnetic cores, typically ferrite, which are highly reliable and long lived. In the past decade, this type of core has been used in computer memories in ever increasing numbers; core failures are nonexistent.

The feasibility of using all-magnetic circuit techniques to realize a digital data-handling system, specifically a PCM telemetry system, was investigated in the first phase of this project. In that study it was found that all of the functions required of a telemetry system could not be realized with then existing all-magnetic circuits. New all-magnetic circuits to realize these functions and provide certain advantages over known circuits were conceived and tested. Based upon these circuits, a logic design for a representative PCM telemetry system was made. The logic design, together with the circuits upon which it was based, has been described in detail in the Phase I Report.[1]

The design arrived at in Phase I was the starting point for Phase II, which had as its final goal the construction of the feasibility breadboard model of this system, which is the subject matter of this Phase II report. The logic design, the circuits and a description of their operation to achieve the required functions used in the feasibility breadboard are described in the following sections of this report, primarily with respect to the differences from the Phase I design. The problems encountered--and some have been formidable--are not recounted in detail

[1] C. H. Heckler, Jr., and J. A. Baer, "PCM Telemetry: A New Approach Using All-Magnetic Techniques," Phase I Report, prepared for National Aeronautics and Space Administration, Langley Research Center, Langley Station, Hampton, Virginia, SRI Project 4687, Contract NAS 1-3380 (June 1964). Also available as NASA CR-229 (May 1965).

here in favor of providing a more complete and uninterrupted exposition of the operation of the feasibility breadboard. Although only sketchy mention is made here of the problems encountered, they have provided direction in formulating the recommendations given in the final section.

II SUMMARY

During the first phase of this project, the application of all-magnetic circuit techniques to PCM-telemetry was investigated. Certain functions had not previously been realized using all-magnetic circuits. In the first phase, the realizability of these functions had to be determined. All-magnetic circuits capable of performing these functions compatibly, compactly, and efficiently were conceived and tested. Based on these circuits, a logic design of a 12-channel PCM telemetry system was prepared. The specifications of this system permitted demonstration of the feasibility of using all-magnetic circuits to realize diversely constituted telemetry systems.

In the second phase, a feasibility breadboard was constructed. During the course of this phase, investigations were conducted in topics relating to the breadboard system, including packaging methods for logic circuits, circuit testing, investigation of the characteristics of magnet wire insulation, methods of insulation removal, and testing of logic blocks. Some of these investigations led to changes in logic that resulted in a reduction in both the system power consumption and the number of components.

Delays occurred in the delivery of the cores, followed by protracted fabrication time for both the mechanical assemblies and wiring of the magnetic circuits. Additional delays occurred when circuits had to be refabricated due to shorting. Finally, partial system testing revealed inadequacies of the mechanical design.

III DESCRIPTION OF FEASIBILITY BREADBOARD

In this section of the report we describe the electrical operation of the breadboard. This section is divided into three parts. The first of these is an overall view of the breadboard, the second describes the logic structure, and the third part describes circuit operation. In this section of the report, emphasis is placed upon those parts of the breadboard that differ from the system conceived during Phase I.

A. Introductory Description of System

The feasibility breadboard is a first model of a PCM telemetry system, sans transmitter, for spacecraft application. The purpose of this breadboard is to demonstrate the application of all-magnetic techniques to PCM telemetry system realization. As such, this model is not directed toward a specific telemetry requirement; rather, it is intended to fulfill requirements that are representative of a class of telemetry specifications. The input to the system we are dealing with consists of the outputs from various sensors. For the analog channels, the sensor output is an analog signal to be converted into its binary representation. The output of this system is this binary representation for each sensor, and it appears in the form of voltage pulses in time sequence.

A system block diagram is shown in Fig. 1. The top row of three blocks comprise the path for information flow, and the remainder of the blocks comprise the control portion of the system. The control portion of the system comprises a timing pulse generation section, a channel commutation section, and a weight current generation section.

The timing pulses are generated by the clock drivers designated by L's and D's on the block diagram. Each of the drivers except D_0 generates a complex pulse pattern as its output; this output is indicated by an arrow or by a group of arrows emanating from each driver block. Each

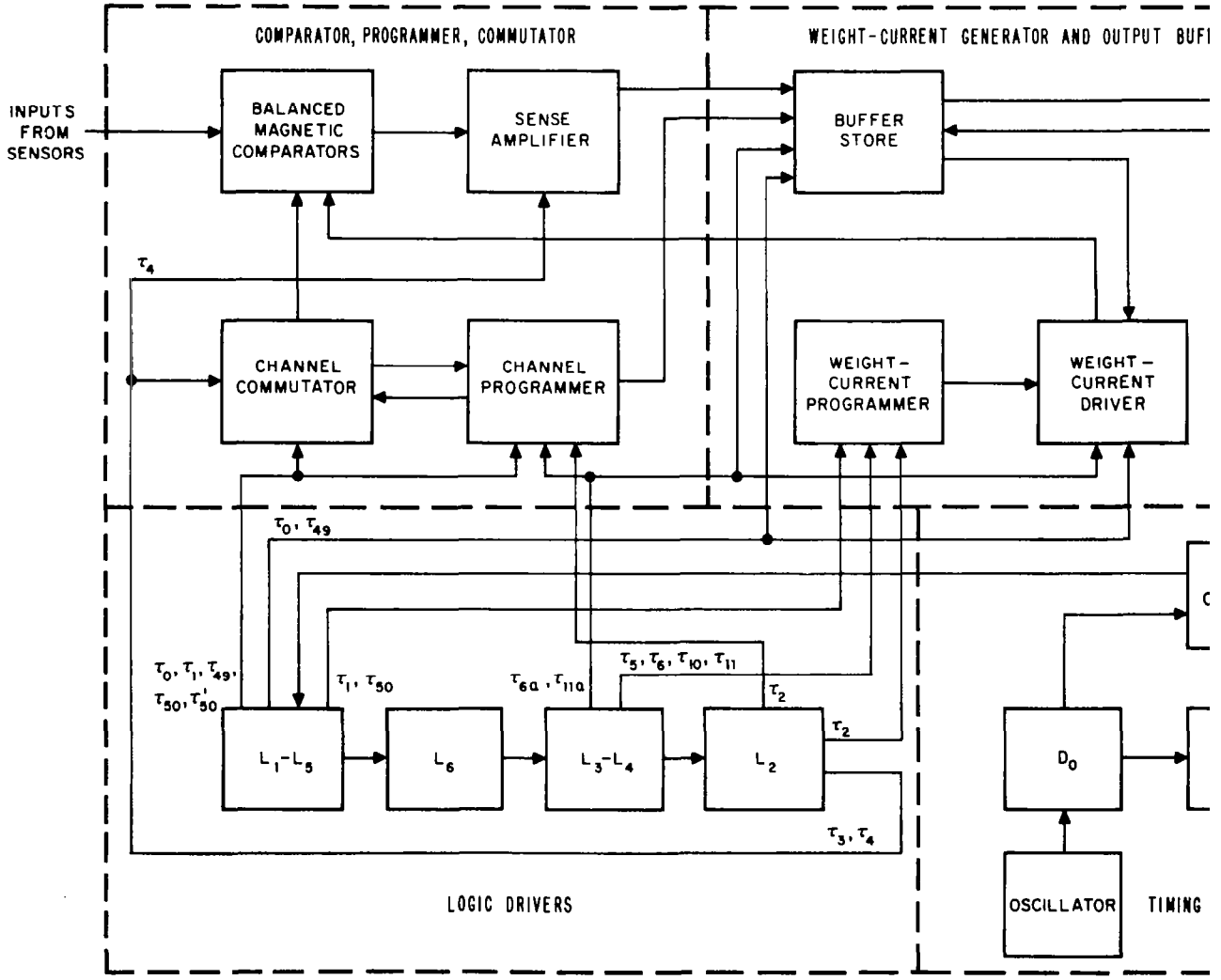


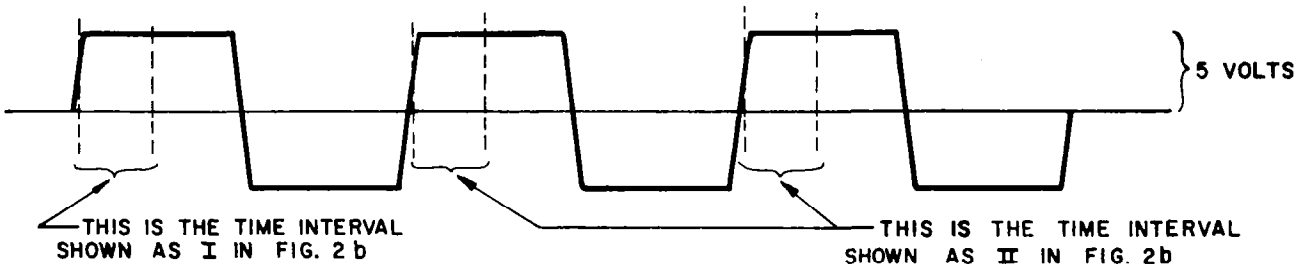
FIG. 1 BLOCK DIAGRAM OF 12-CHANNEL PCM TELEMETRY FEASIBILITY MOD

driver (except D_0) requires a trigger current-pulse for its input; this trigger input is indicated by an arrow terminating at the driver block.

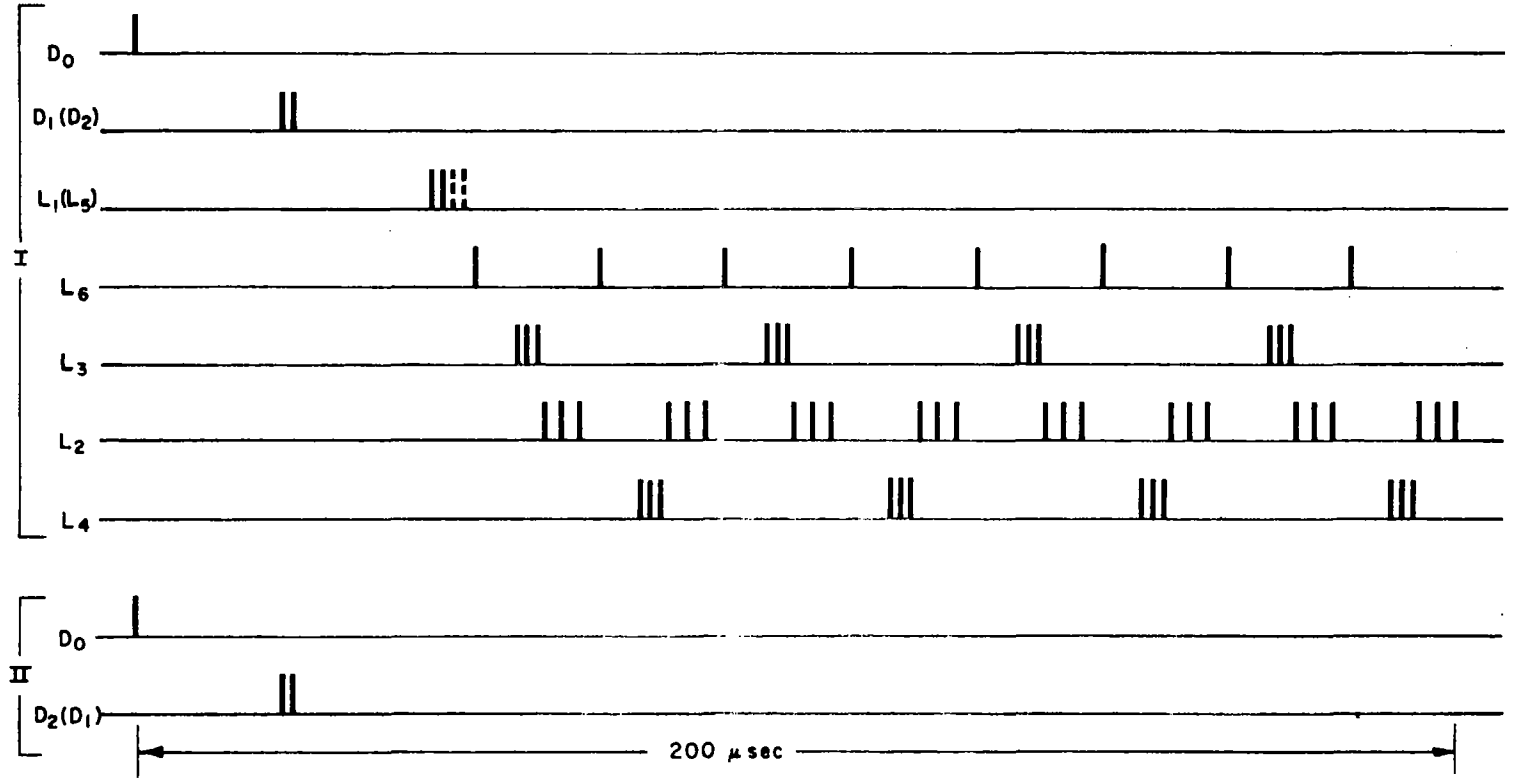
The system timing pulses are illustrated in the diagrams that form Fig. 2. The set of pulses identified by I occurs in one of two forms once every seventh cycle of the oscillator output. One form occurs when drivers D_1 and L_1 generate the pulses indicated on rows 2 and 3 (from the top) and another form occurs when drivers D_2 and L_5 generate these pulses. The set of pulses identified by II occur once during each oscillator cycle with D_1 and D_2 alternating, except for those cycles that initiate the generation of Pulse Set I.

The commutation of twelve information channels and two synchronizing channels is effected by the blocks labeled Channel Commutator and Channel Programmer. These circuits are implemented by all-magnetic logic techniques, in particular, the "stopper" logic circuits that have been developed as a part of this project. The fourteen channels (as identified in Fig. 5) are sampled in the following sequence: 1, 2, 3, 4, 5, 6, A, B, 1, 2, 3, 4, 5, 6, C, D, 1, 2, 3, 4, 5, 6, E, F, 1, 2, 3, 4, 5, 6, Sync 1, Sync 2. The composite circuits which are located in the cavity block (the housing for a group of stopper circuits) labeled (A) in Fig. 3 and labeled on the photograph of the breadboard, Fig. 4, provides the commutation functions indicated by the commutator block in Fig. 1. These same composite circuits and the logic circuits located in cavity block labeled (B) in Fig. 4 provide the programming functions indicated by the channel programmer block in Fig. 1.

This system accommodates a random mixture of high- and low-level input signals and a mixture of digital and analog input signals. Analog-to-digital conversion is effected by the successive approximation technique, which is implemented by the weight current programmer, cavity block (D), and store, cavity block (E). Each channel has a null-sensing device called a balanced magnetic comparator, or BMC. The comparators are located within the composite circuits in cavity block (A) of Fig. 4 and the sensors are connected directly to the BMC of the appropriate composite circuits. Analog signal amplification is not required because the comparator output is digital.



(a)



(b)

FIG. 2 SYSTEM TIMING PULSES
(a) Oscillator Pulses
(b) Drive Pulses

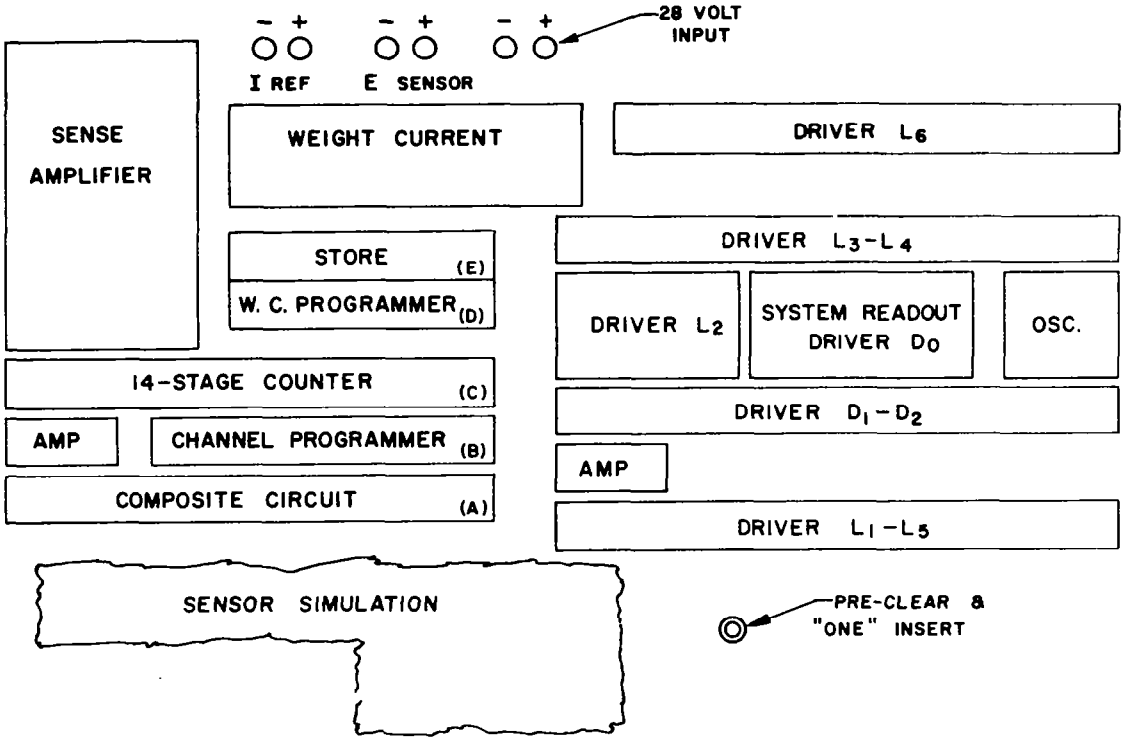


FIG. 3 BREADBOARD LAYOUT AND IDENTIFICATION OF CIRCUITS

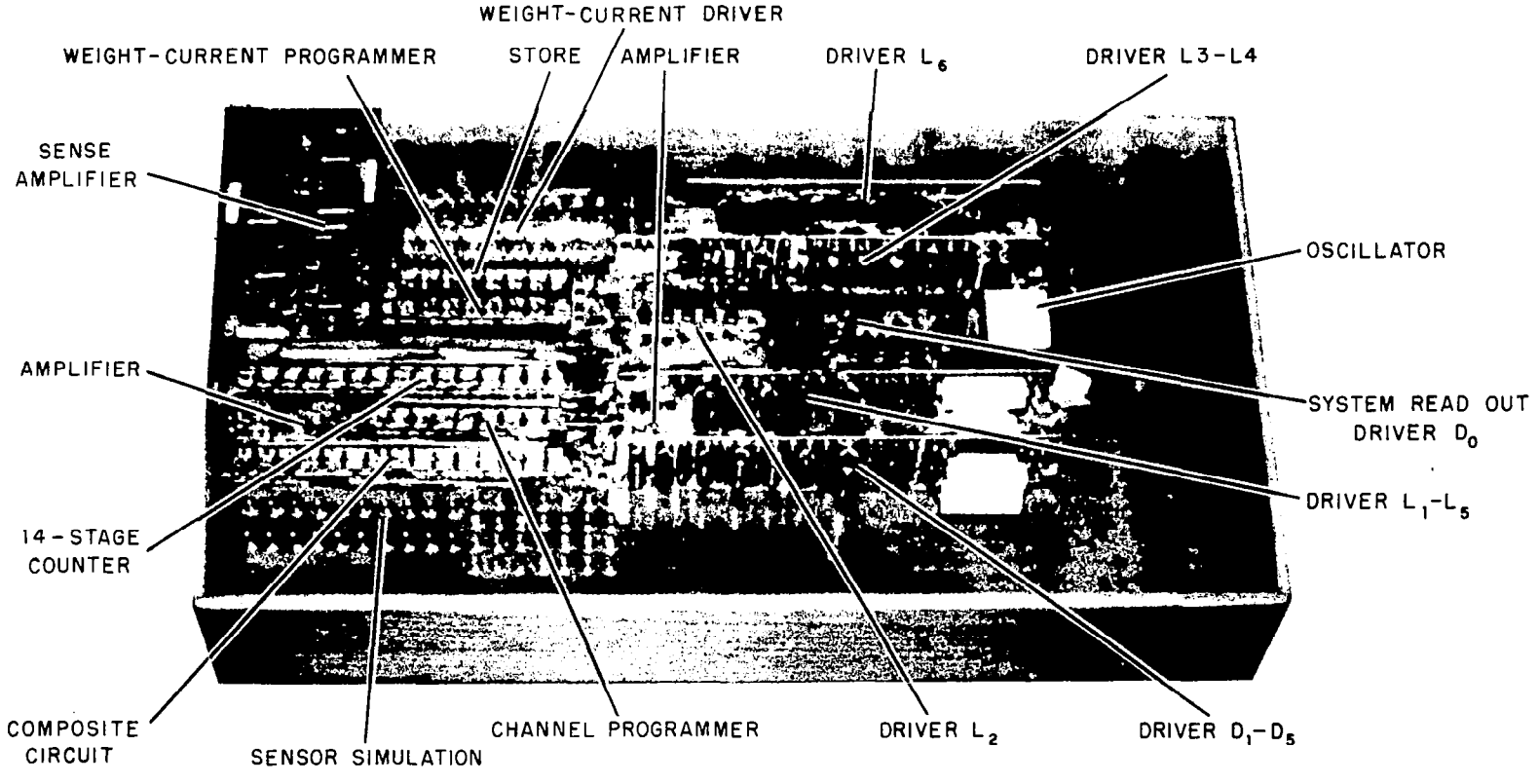


FIG. 4 PHOTOGRAPH OF FEASIBILITY BREADBOARD

The output of the system is provided through readout of the buffer store, under the control of the 14-stage counter, cavity block (C), at a 500 bit per second rate derived from the 500-cps tuning fork oscillator. The system output occurs in synchronism with the output pulse from D_0 shown in Fig. 2(b).

B. Logic Description of Feasibility Breadboard

The logic design of the feasibility breadboard is basically the same as that made in Phase I; certain modifications have been made to reduce the system power and number of components. Other changes have been made as more detailed data on the performance of the circuits indicated the desirability of such a change. The logic design of the feasibility breadboard is described in this section by functional block with particular emphasis on the differences from the Phase I design.

1. Timing Generation Circuits

The logic for this section has been simplified from that of the Phase I design and is shown as the timing generator block in Fig. 5. This has been in large part a result of the experimental work undertaken in this phase on the multipulse driver. It was found that the required burst of (eight) pulses necessary for digitizing could be generated simply by an extension of one of the early multipulse driver designs. The present logic (system) design uses a low-frequency oscillator, since the gating of high-frequency pulses to effect the digitizing is no longer required. A reduction in system power consumption, a reduction of 20 logic stages, and a net reduction of five multipulse drivers have resulted from the changes.

The primary timing source is a 500-cps tuning-fork oscillator. The output of this oscillator is fed into driver D_0, which amplifies and shapes this signal into a 3-μsec pulse. This pulse provides the trigger input to drive multipulse drivers D_1 and D_2 and also provides the system output read drive at the system output bit rate.

The 14-stage ring counter provides the seven-bit read pulses τ_{42} through τ_{48}, which read out each of the seven bit locations in the buffer

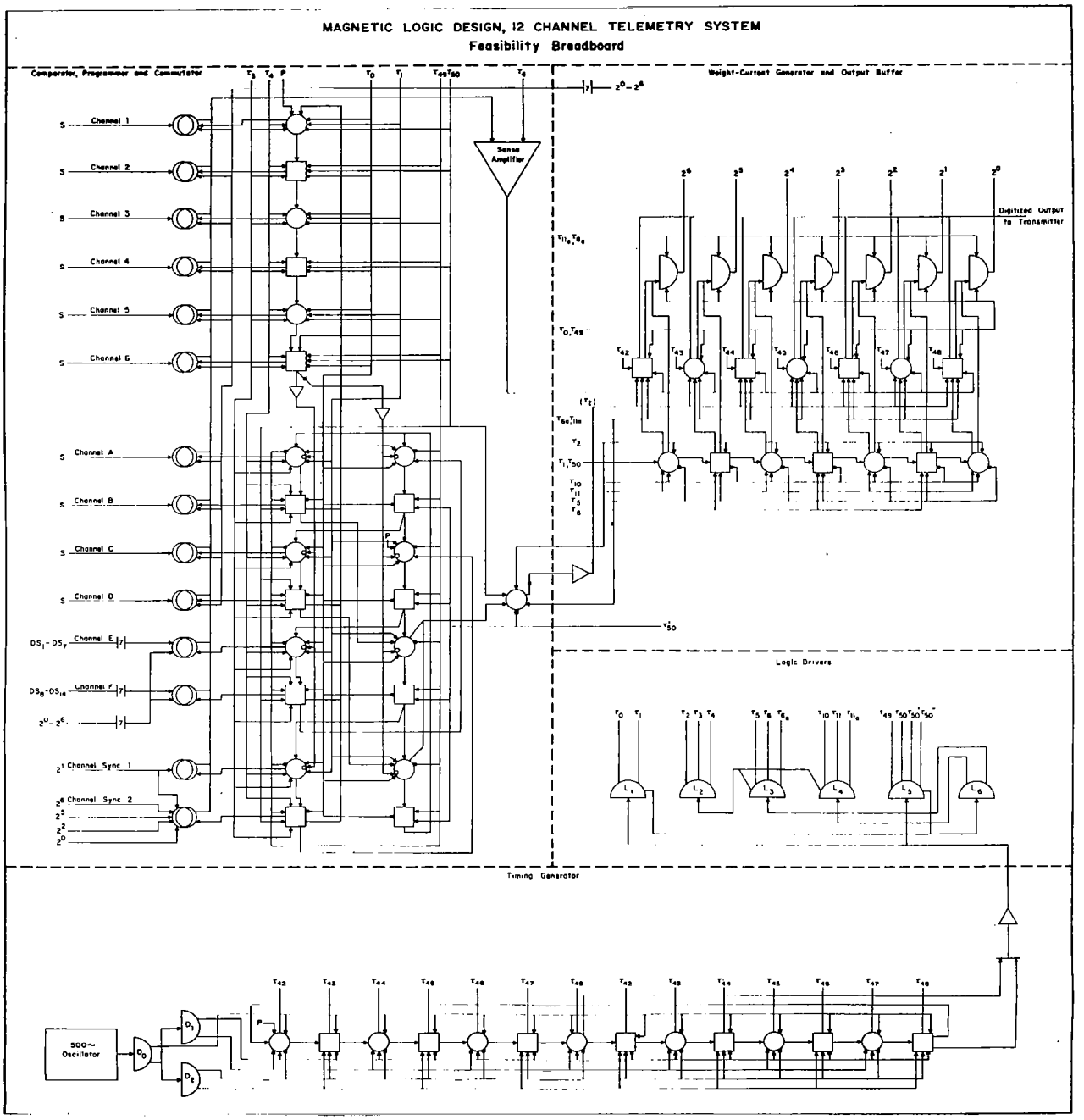


FIG. 5 LOGIC DIAGRAM OF FEASIBILITY BREADBOARD

store. A bit-read pulse is produced from the stage holding the single ONE contained in the register at the time the system output read drive is applied to all stages. As the ONE propagates along the register, the bit-read pulses are produced in sequence. Two complete sequences are produced by the ONE propagating through all 14 stages.

An additional type of output is produced by this counter following every seventh bit-read pulse (τ_{48}). This output determines the time for commutating from one channel to the next. After it has been amplified by the interface amplifier it provides the input for the multipulse drivers L_1 and L_5, which accomplish the actual commutation. Although logically only seven pulses--and hence a seven-stage ring counter--are required, the magnetic circuits require that a ring counter contain an even number of stages in order to maintain a stable pattern. For this reason, the ring counter is 14-stages long and the readout of each bit location in the buffer store is provided from either of two of the stages, seven stages distant.

An output from either driver L_1 or L_5 provides the input for driver L_6. L_6 is a multipulse driver designed to produce eight sequential pulses. This burst of pulses provides the basic timing interval for digitizing and triggers drivers L_3 and L_4 which in turn triggers L_2. These three drivers produce the drive currents used in this process.

2. Channel Commutation

Channel selection is accomplished by setting one of the composite circuit logic stages into the ONE state, thereby selecting the output from the sensor associated with that stage to be digitized. These stages are the column of 14 logic stages--the super and prime channel stages--located in the comparator, programmer, and commutator block of the logic drawing Fig. 5. The interlocking circles associated with each stage form the logic symbol for the BMC, which is physically included in the stage that is referred to as the composite circuit.

Channel commutation is accomplished by transferring the ONE into the next super or prime channel stage, as determined by the program. The actual transfer is effected by the drive pulses from multipulse

drivers L_1 and L_5. The programming for the super channels is invariant and determined by the wired connections. They are always commutated sequentially from the first through the sixth channel. The prime (and sync) channels are commutated in pairs, under control of the prime channel programmer (the column of eight stages in the same block of Fig. 5) to provide the desired channel commutation sequence. The prime channel programmer controls the selection of the appropriate pair of prime channels by circulating a ONE in synchronism with the ONE sequencing through the super-channel stages. When the ONE is transferred out of the sixth super-channel stage, the inhibit amplifier is turned on. This prevents the normal transfer of the ONE in the prime channel programmer; instead the ONE is transferred to an odd prime-channel stage. Note that there are two outputs associated with each even stage of the prime-channel programmer; one to the succeeding odd stage and the other to one of the odd prime-channel stages. In the absence of an input to the inhibit amplifier, a ONE in an even stage is transferred to the odd stage of the prime channel programmer. The occurrence of an input to the inhibit amplifier directs the ONE transfer to the odd prime channel stage instead.

At this time only a single ONE is contained in the super, prime channel, and prime channel programmer stages. It is in an odd-prime-channel stage, having been transferred there from the prime-channel programmer. The transfer of the ONE out of the sixth super-channel stage has removed the ONE from the super-channel stages.

The adjacent even prime-channel stage is selected at the next commutation time. At the following commutation time the ONE is transferred out of this even prime-channel stage setting a ONE into two stages connected to its output: the first super-channel stage and one of the odd prime-channel-programmer stages. The output of each even prime channel stage is connected to provide a ONE transfer to only one of the odd prime channel programmer stages. The stages are arranged such that after the ONE is reinserted in the prime channel programmer it is advanced two stages relative to its position had prime channel selection not occurred.

As before, the ONE in the prime channel programmer is cycled in synchronism with the ONE sequencing through the super channel stages. Again as the ONE is transferred out of the sixth super channel stage, the normal transfer of the ONE from the even to the odd stage in the prime channel programmer is inhibited, and the ONE is transferred into the associated odd prime channel stage. Note that at this time the even prime channel programmer stage from which the ONE is transferred is located two stages in advance of the stage from which the previous transfer occurred, and the prime channel stage receiving the ONE is two stages in advance of that previously selected. In a like manner remaining prime and sync channels are selected to complete (and then repeat) the commutation program.

3. Analog-to-Digital Conversion

The measurand is converted to its digital representation by the method of successive approximations. The departure from a conventional logic design for this function arises from the use of a separate, simple null detector--the balanced magnetic comparator circuit--with each channel. To accomplish the conversion to seven bit accuracy, seven pairs of drive pulses, a pair (τ_3, τ_4) associated with each weight, are applied to the BMC circuit. These pulses are supplied from driver L_2, a transistorized driver. The drive pulses are applied to all channel stages simultaneously. The selection of a channel, by setting that stage in a ONE state, permits the application of these drive pulses to the BMC associated with that channel. All other channel stages which are in the ZERO state block the application of the drive pulses to the BMC circuits associated with each of them. The output from a BMC circuit resulting from a comparison of the measurand and weight(s) is digital: bit indication is by polarity, a positive polarity representing a logic ONE--the measurand greater in magnitude than the weight(s). The measurand input to the BMC circuit derives directly from the sensor and, as the output is digital, the requirement for linear amplification and manipulation of analog signals is eliminated. The case of a match condition, where an output signal is not developed, is treated as a ZERO. The output

from all 14 BMC circuits--the BMC is also used in the digital and sync channels--are connected in a logic OR to the input of the sense amplifier, which in turn causes a ONE to be transferred into the buffer store.

In this breadboard the digital sensors associated with each digital channel are simulated by switches. For the two sync channels, switches are also used to permit insertion of any 14-bit code. Seven cores are interposed between the sensors (switches) and the BMC for each digital or sync channel. The sequential selection of each of the weights causes one out of the seven cores in each of these channels to produce a measurand current dependent upon the state of the sensor. The occurrence of such a measurand current in the selected channel produces a ONE output signal from the BMC associated with that channel. This signal, as in the analog channels, causes a ONE to be set in the store. Thus the seven weights provide the read out of seven digital sensors per channel.

4. Weight-Current Generation

The use of the BMC circuit requires current inputs, specifically, a measurand current and weight currents. The weight currents must be obtained from a high-impedance source in order to maintain precision under varying load conditions. Digitizing to seven-bit accuracy is accomplished by the method of successive approximation. To accomplish this, the current drivers are required to be turned on in both a sequential and a repetitive manner. Each driver is turned on, initially, in a sequential manner, under control of the weight-current programmer. Each stage of the programmer controls the turn-on of one driver. The repetitive turn-on of these drivers is under the control of the buffer store. Each bit storage location controls the turn-on of one driver. Each driver then, is able to be turned on either by the programmer or the store. The sequential turn-on is effected by inserting a ONE in the first stage of the weight-current programmer, and then advancing the ONE through the seven stages of the programmer. The presence of the ONE in a stage permits transmitting the weight current drive clock, τ_2, through the stage to turn on the weight-current driver associated with that stage.

The weight current drive clock is applied simultaneously to all stages of the weight current programmer, but it is blocked by the stages containing a ZERO, and so does not effect the turn-on of any but the selected driver. The advance of the ONE along the register turns on the drivers in sequence. This sequential turn-on occurs for both the analog and digital channels.

The repetitive turn-on of the drivers is effected by the presence of a ONE in one of the bit stages of the store. As in the weight-current programmer, the presence of a ONE permits the transmission of the weight-current drive clock [here applied through the digit channel detector amplifier and referred to as (τ_2)] through the stage to turn on the weight-current driver associated with that stage. A restore pulse (τ_{6a}, τ_{11a}) is applied after termination of the weight-current pulse. The next occurrence of (τ_2), the weight-current drive clock, is again transmitted through this stage and turns on the same weight-current driver. Both (τ_2) and τ_{6a}, τ_{11a} are applied to eacn bit stage in the store; thus, it is seen that once a ONE is inserted into a bit stage of the store, the driver associated with that stage will be turned on by each subsequent weight-current drive clock until the digitizing process for that channel is complete.

The store serves the additional function of a time buffer between the digitizing bit rate and the system output bit rate. Each bit location in the store is read out from two stages in the 14-stage counter in the timing generator. After the full word has been read out of store it is cleared at the time the next channel is commutated.

C. Operational Description of Feasibility Breadboard

This portion of the report deals with the feasibility breadboard at the circuit and component level. We point out here extensions that have been made to the basic circuits, the basic circuits having been described in the Phase I report. Certain other operational details are also included. Schematic diagrams of the circuits are contained in this section.

1. Timing Generator Circuits

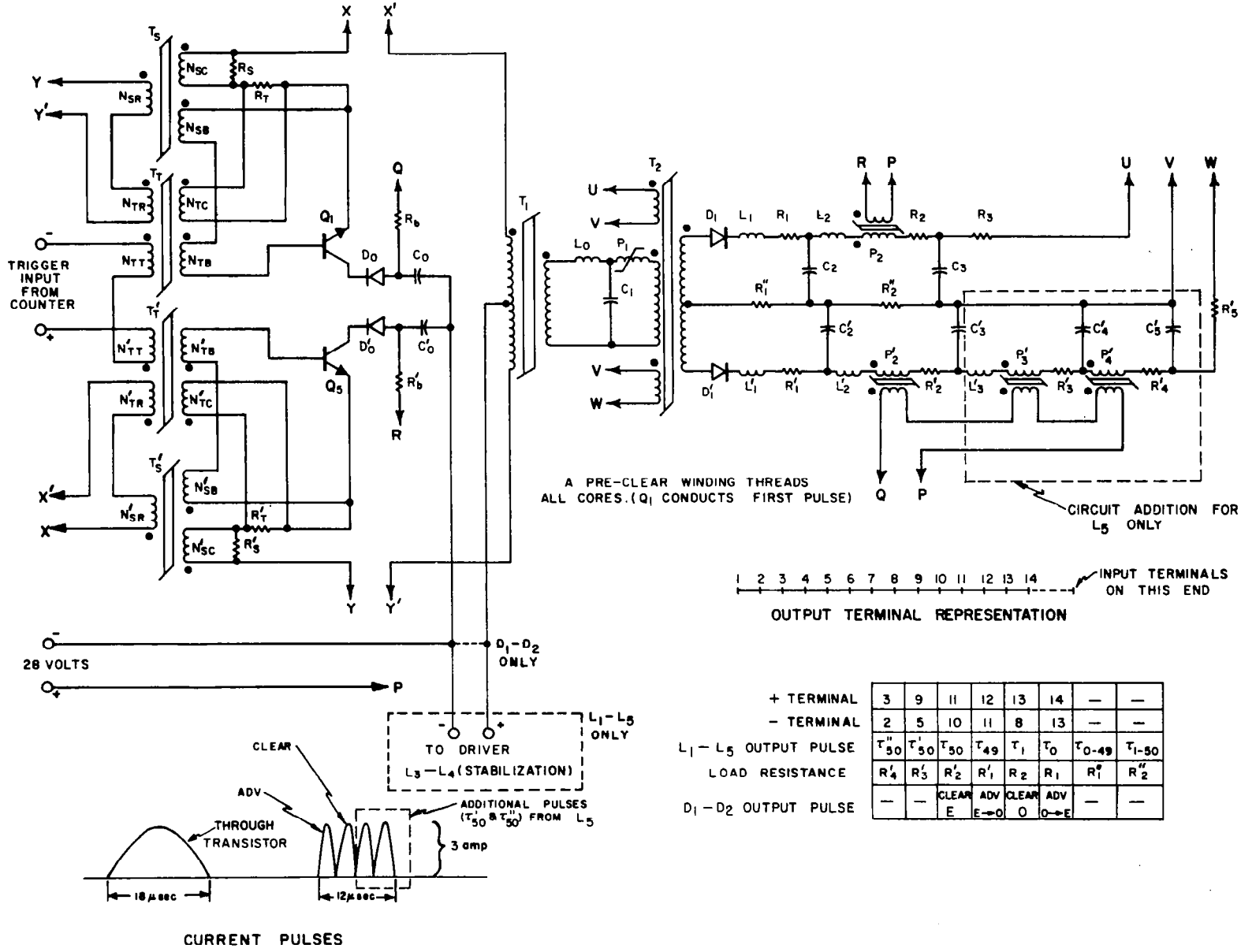
The generation of the pulse sequences needed in this system is controlled by the oscillator, the ring counter, and the clock drivers. The drivers are an integral part of this control function, first, because certain drivers are triggered by other drivers through frequency dividing circuits and a type of frequency multiplication, and second, because the drivers generally produce a set of output pulses having prescribed time relationships to others within the pulse set.

The master clock for this system is a tuning fork oscillator. The particular kind used in the breadboard is Bulova American Time Products Type 32. It provides a 5v peak quasi-square wave into a 20 kilohm load, and its frequency of 500 cps is accurate to within ±0.1 percent. The driver D_0 is triggered on the leading edge of the positive-going portion of the waveform to initiate the series of timing pulses.

Driver D_0 has a single output pulse, which triggers the multipulse drivers D_1 and D_2 through a divide-by-two circuit. The division is accomplished by using square-loop cores in the trigger input circuit and selectively resetting these cores. In Fig. 6 the trigger cores are labeled T_T and T_T'.

The square-loop transformers labeled T_1 and T_2 in Fig. 6 serve two functions. First, they provide the necessary impedance transformation that permits operation of the entire system from a single power supply voltage. Second, they permit a portion of the circuit to be shared by both driver D_1 and driver D_2. This common portion of the circuit, comprising inductor L_0, the capacitor C_1, and pulsactor P_1 is operated in a bipolar manner as a result of combining D_1 and D_2, and this automatically provides for the resetting of pulsactor P_1.

The current-pulse through the transistors Q_1 and Q_5 is 18 μsec wide, as pictured in the figure. This pulse is compressed by circuit action into 3 μsec to give the desired output pulse width. The 3-amp, 3-μsec output pulse would necessarily be reflected by the transformers T_1 and



+ TERMINAL	3	9	11	12	13	14	—	—
− TERMINAL	2	5	10	11	8	13	—	—
$L_1 - L_5$ OUTPUT PULSE	τ''_{50}	τ'_{50}	τ_{50}	τ_{49}	τ_1	τ_0	$\tau_{0\text{-}49}$	$\tau_{1\text{-}50}$
LOAD RESISTANCE	R'_4	R'_3	R'_2	R'_1	R_2	R_1	R''_1	R''_2
$D_1 - D_2$ OUTPUT PULSE	—	—	CLEAR E	ADV E→O	CLEAR O	ADV O→E	—	—

FIG. 6 MULTIPULSE DRIVER CIRCUIT $D_1 - D_2$ AND $L_1 - L_5$

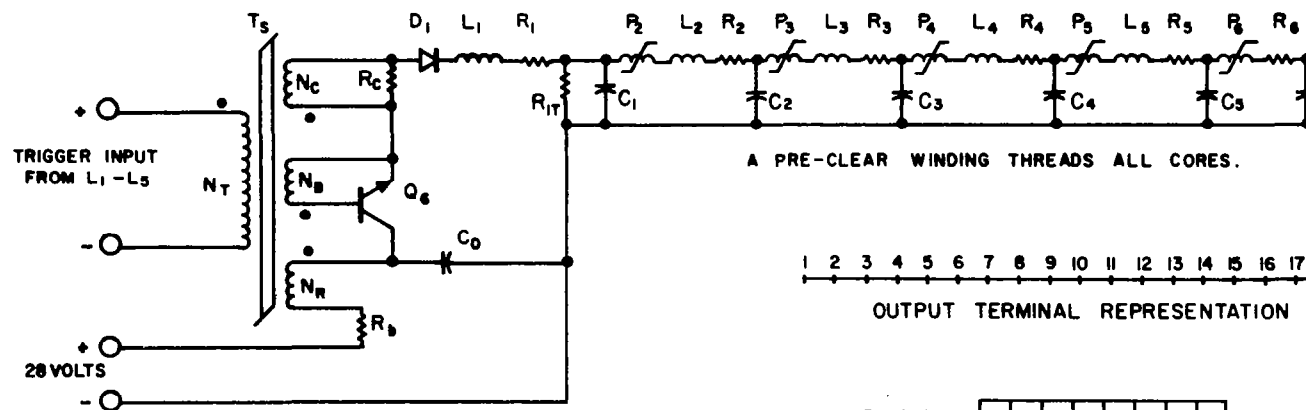
T_2 into the transistor circuit as an 18-amp, 3-μsec pulse if pulse compression were not used. This compression reduces the peak current through the transistor to 3 amp.

The pulsactor windings that terminate in the letters P, Q, and R are so-called "stabilizing" windings that are necessary to provide adequate operating margins. Likewise, the windings labeled U, V, and W on T_2 are stabilizing windings. The function of this stabilization is to place these cores in a known reference state at a specified time in their operating cycle.

Figure 6 shows the schematic for both driver combination D_1 - D_2 and driver combination L_1 - L_5. The difference in the two drivers is noted on the figure by the parts enclosed by the dashed lines. Driver D_1 - D_2 generates a total of four output pulses while L_1 - L_5 generates a total of six output pulses. The two stages associated with P_3' and P_4' in Fig. 6 supply the two additional pulses from L_5.

The driver L_1 - L_5 triggers driver L_6; the latter is shown schematically in Fig. 7. Driver L_6 has only one square-loop transformer in the transistor input circuit because frequency division is not required here--an output pulse group occurs for each input signal. The output is a sequentially ordered group of eight pulses; the purpose of these pulses is to trigger another driver (L_3 - L_4). The generation of these eight output pulses (for triggering) from one input trigger pulse constitutes the frequency multiplication mentioned above. The delay between successive pulses must be greater than a certain minimum (16 μsec). This delay is maintained over voltage and temperature variations by the action of the pulsactor resetting circuit consisting of C_8 and R_{8T}. The transformer T_s is reset during the charging of capacitor C_0.

The 14-stage ring counter in the timing generator section is the link between D_1 - D_2 and L_1 - L_5. D_1 - D_2 is the pulse power source for the ring counter that in turn triggers driver L_1 - L_5 through an amplifier. The ring counter is composed of 14 stopper circuit stages, like the one stage shown schematically in arrow notation in Fig. 8. This stage has two outputs, one from the output-balanced-pair (OBP), and the other from



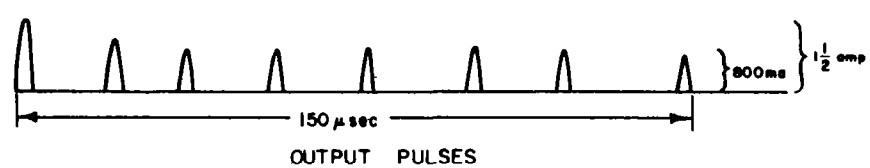


FIG. 7 MULTIPULSE DRIVER CIRCUIT L_6

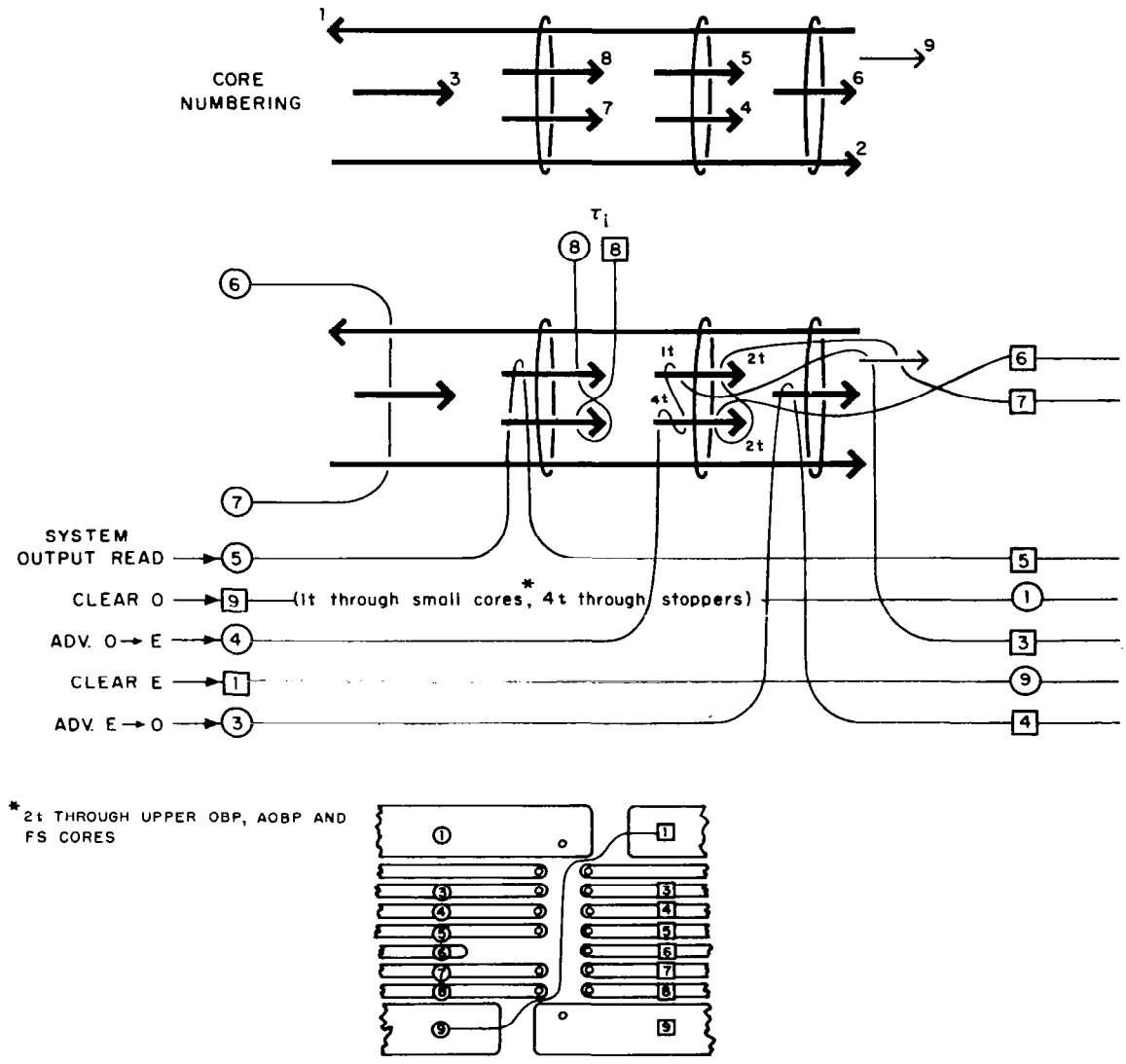


FIG. 8 STOPPER LOGIC CIRCUIT: 14-STAGE RING COUNTER

the auxiliary-output-balanced-pair (AOBP). The OBP is identified as Cores 4 and 5 in the figure and the AOBP as cores 7 and 8. The coupling loop that connects two neighboring stages in the counter links the OBP. The flux change from the OBP in one stage produces a corresponding flux change in the OBP and AOBP of the next stage in a ONE transfer. The AOBP output winding is connected to one stage in the buffer store to control the readout of this bit storage location during system read-out.

The transfer out of the OBP must meet certain current and flux gain requirements to obtain bistable circuit operation. Of the several methods for obtaining gain that were described in the Phase I report, turns ratio means have been used here. The output coupling loop links the OBP with two turns while the input winding to the next stage has only a single turn. This provides the necessary flux gain, and a clipper core (Core 9) reduces the flux transfer for low levels of flux. The clipper core is linked by the output coupling loop and is driven by a clock pulse to "clip out" a certain amount of flux at each transfer time. Current gain is effected by using multiple turns on the drive winding linking Core 4 of the OBP. This core is driven in the clear direction at transfer time so it can be driven with a high amplitude mmf. These same gain circuits are used with the AOBP.

2. Channel Commutator Circuits

Schematic drawings for the super-channel composite circuit, the prime-channel composite circuit, and the prime-channel programmer circuit are given in Figs. 9, 10, and 11, respectively.

The composite circuit consists of a balanced magnetic comparator and a stopper logic circuit. In the super-channel composite circuit, the OBP of one stage is connected to the adjoining stage in the cavity block as it is in the 14-stage ring counter. This wired transfer from one stage to the next constitutes the programmer function for the super channels and is invariant. Prime-channel programming is effected by wired transfer only for pairs of channels.

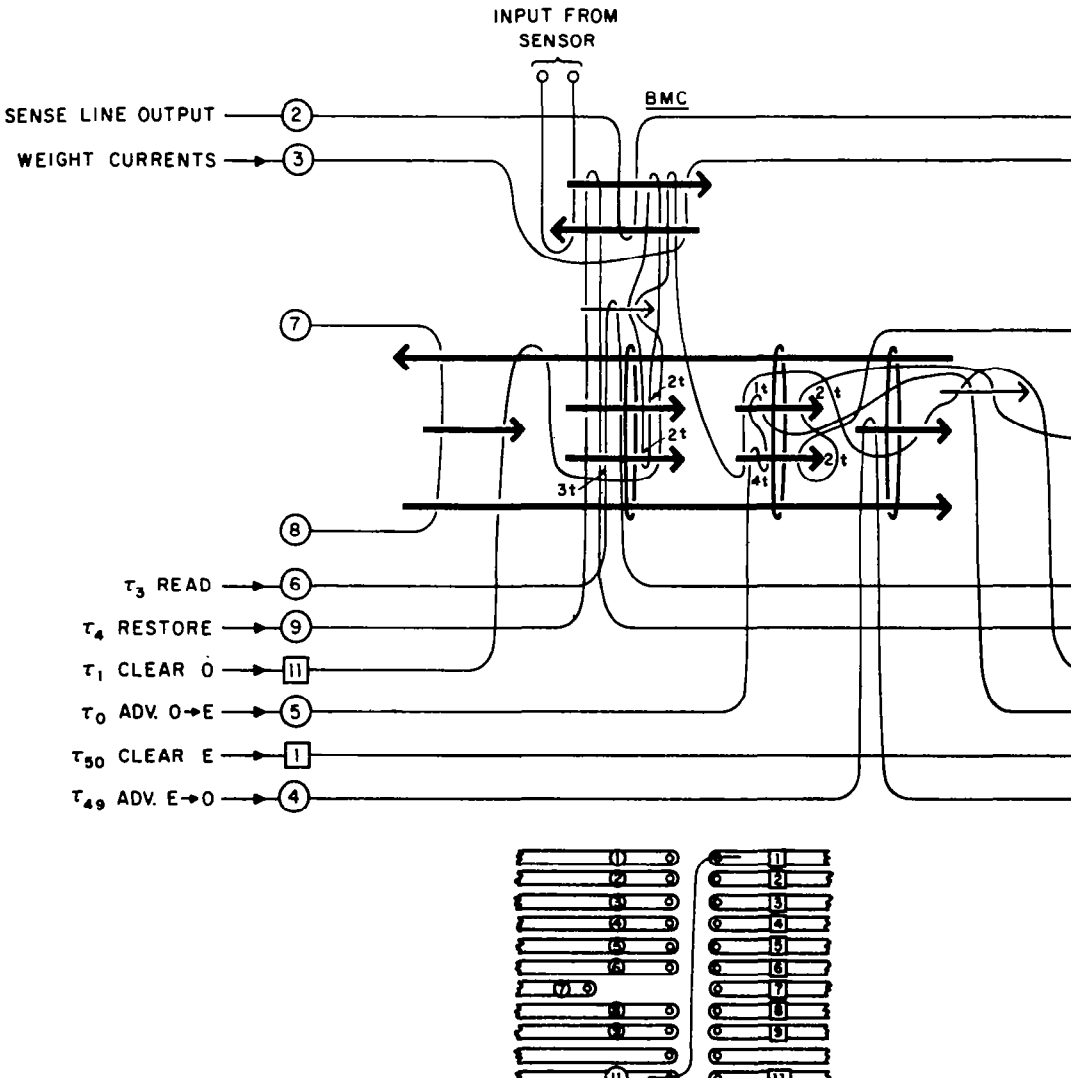


FIG. 9 STOPPER LOGIC CIRCUIT: SUPER CHANNELS

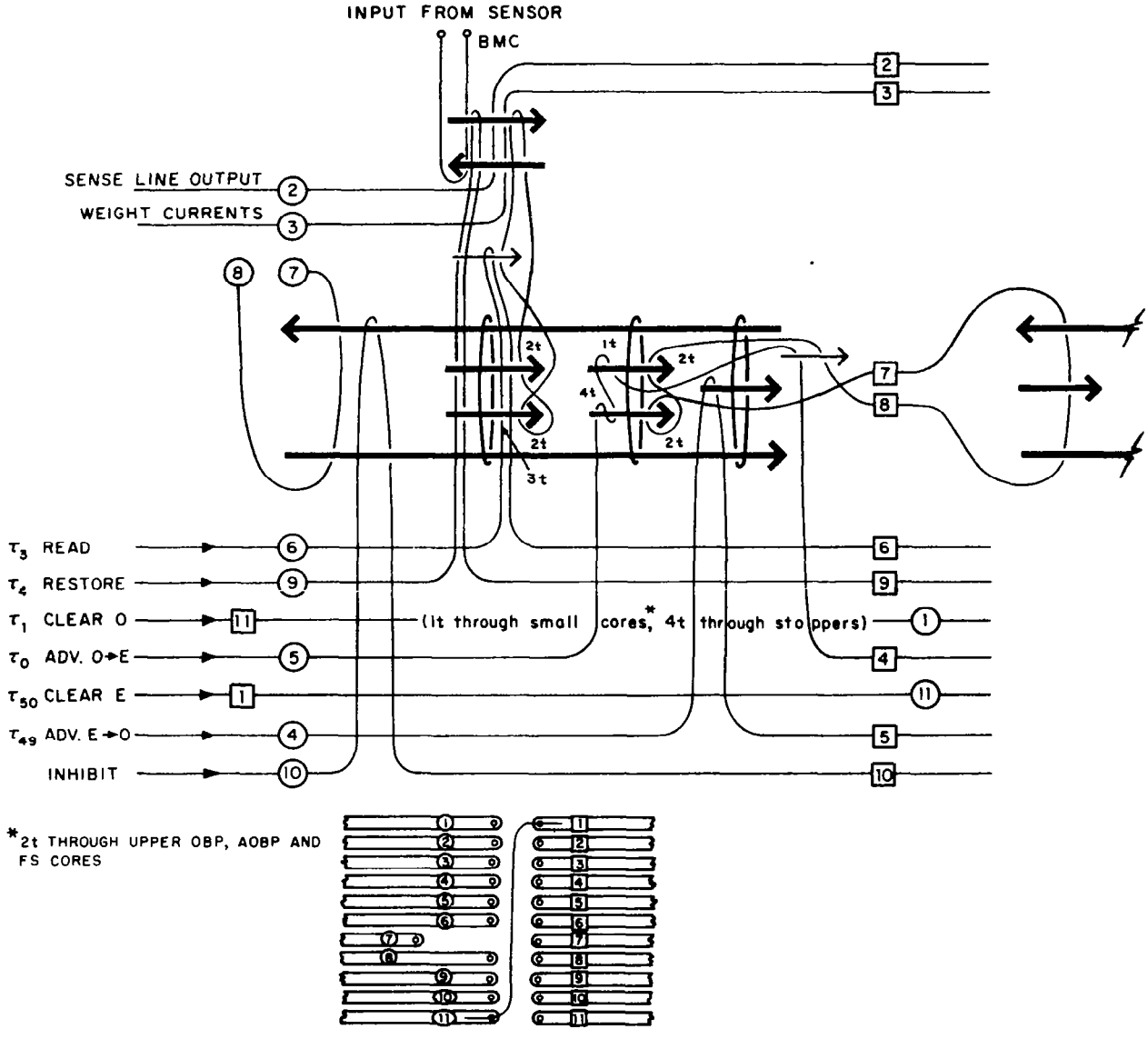


FIG. 10 STOPPER LOGIC CIRCUIT: PRIME CHANNELS

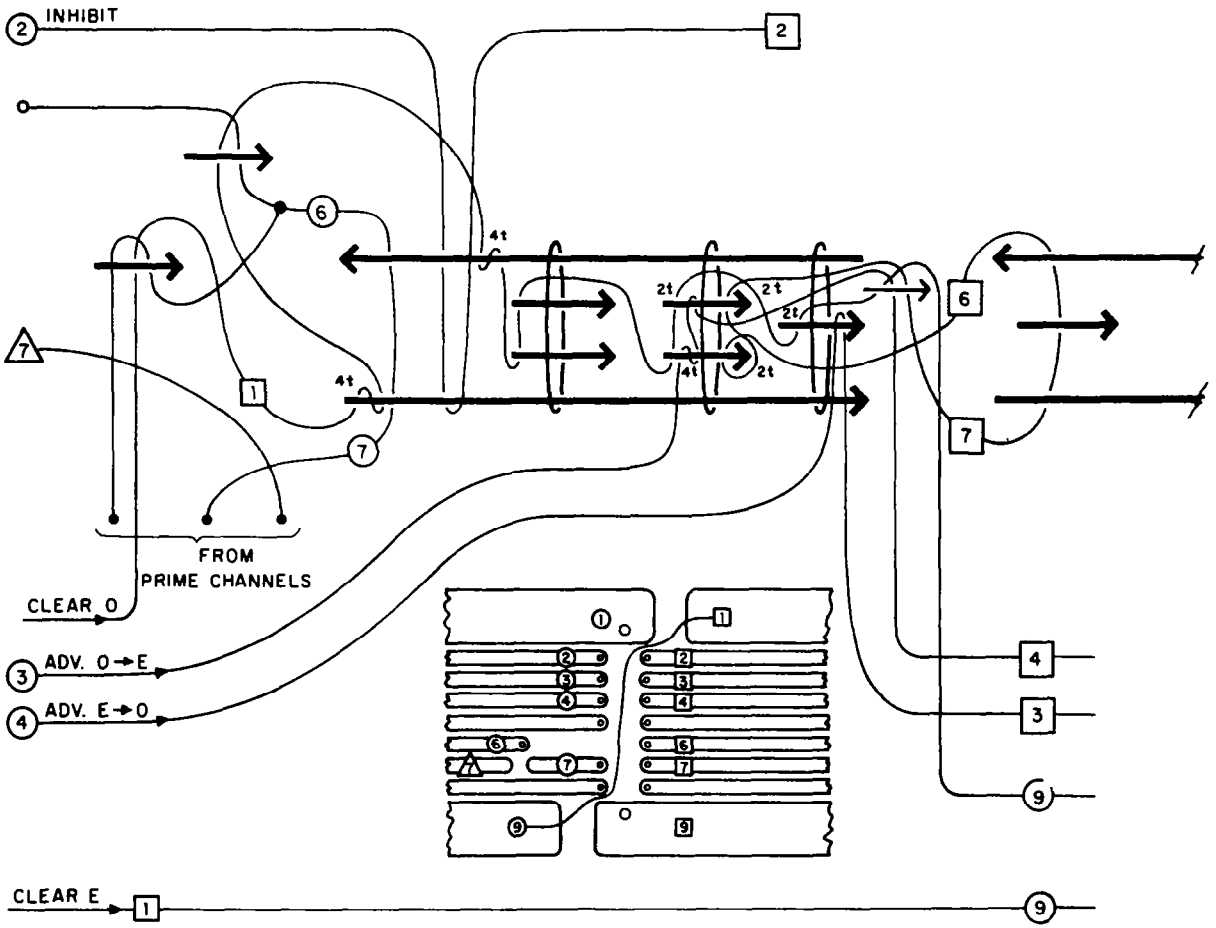


FIG. 11 STOPPER LOGIC CIRCUIT: PRIME CHANNEL PROGRAMMER

The output from the sixth stage of the super-commutated channel is directed to one of four possible channels under the control of the prime-channel programmer, Fig. 11. The OBP from this sixth stage drives an inhibit amplifier with two outputs, one an amplified version of the input and the other a NEGATION output. These outputs are used to select either the prime channel stages or the prime channel programmer stages into which a ONE transfer can be made when transferring from an even stage of the prime channel programmer. The coupling loop from this even programmer stage is coupled into two stages by a series input connection. The selection is done by action of the inhibit amplifier that inhibits the transfer either into the prime channel programmer stages or the prime channel stages. Inhibiting consists of passing current through the stopper cores in a sense opposite to that of the current in the coupling loop during ONE transfer. (The winding from Terminal 2 in Fig. 11 is an inhibit winding.)

3. Analog-to-Digital Conversion Circuits

The input circuit to a balanced magnetic comparator consists of a winding linking both cores as indicated in Figs. 9 and 10. For prime channels A and C this winding consists of one turn on each core to effect the minimum channel sensitivity. This is likewise true for the digital and sync channels. Prime Channels B and D have a 5-ma full-scale sensitivity and therefore have a 20-turn input winding on each core. All the supercommutated channels (1 through 6) have the maximum sensitivity and therefore have 100-turn input windings.

The BMC forms a part of the composite circuits shown in Figs. 9, and 10. The flux source for the comparator is the AOBP. In the testing done in Phase I of this contract, a single toroid was used as the flux source; here a balanced pair of cores is used. In the loop connecting

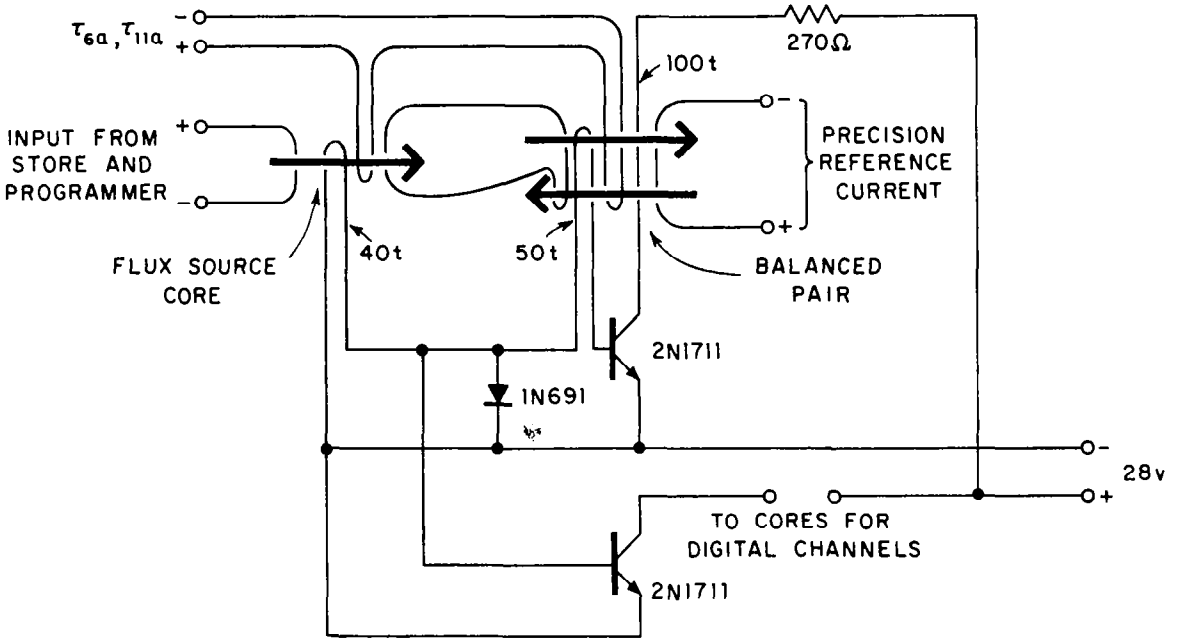
For each of the seven comparisons required in the digitizing process, the read and restore pulses, τ_3 and τ_4, first switch and then clear the BMC of the selected channel. An unbalance in the flux switched in the BMC by τ_3 is produced by the presence of unequal measurand and weight currents. The direction of this unbalanced flux is determined by the relative magnitude of the inputs and determines the polarity of the output from the BMC produced by τ_4 clearing the circuit. The polarity of the output then identifies the input of greater magnitude. Pulses τ_3 and τ_4 are each 2.5-μsec pulses and both occur during the interval that the weight currents are present.

The transistorized sense amplifier senses a positive polarity signal greater than a threshold value and provides a 3-μsec output pulse, which is used to insert a ONE in the store.

4. Weight-Current Generator Circuit

The weight-current drivers generate flat-topped precision current pulses of 6-μsec duration. The amplitude of the pulse is controlled through the use of a modified BMC circuit and a reference current. The weight-current driver circuit shown in Fig. 12 differs from the basic circuit discussed in the Phase I report in two respects. First, the diode in the base emitter circuit clamps the voltage from the flux source core so that this voltage, which is the turn-on voltage for the driver, is essentially constant during the time that a weight current is being generated. This helps to maintain the flat-topped nature of the current pulse. The second difference is the presence of an additional transistor. This transistor supplies the pulse current used to switch the cores associated with the digital channels, and is required because the lower weights do not have adequate current amplitude to switch these cores.

There are seven circuits such as the one shown in Fig. 12. The number of turns on the precision reference current windings are as indicated in the figure to provide the seven different weight currents. An individual circuit is turned on under logic control. The AOBP (Cores 7 and 8) from a stage of the weight-current programmer and a stage of the buffer store (shown in Figs. 13 and 14) are linked by a series winding



CORES:
AMPEX 802-40
1 TURN WINDINGS UNLESS OTHERWISE INDICATED

WEIGHT	TURNS ON REFERENCE CURRENT WINDING	REFERENCE CURRENT, ma
64	32	100
32	16	100
16	8	100
8	38	10
4	28	10
2	18	10
1	25	1

FIG. 12 WEIGHT-CURRENT DRIVER CIRCUIT

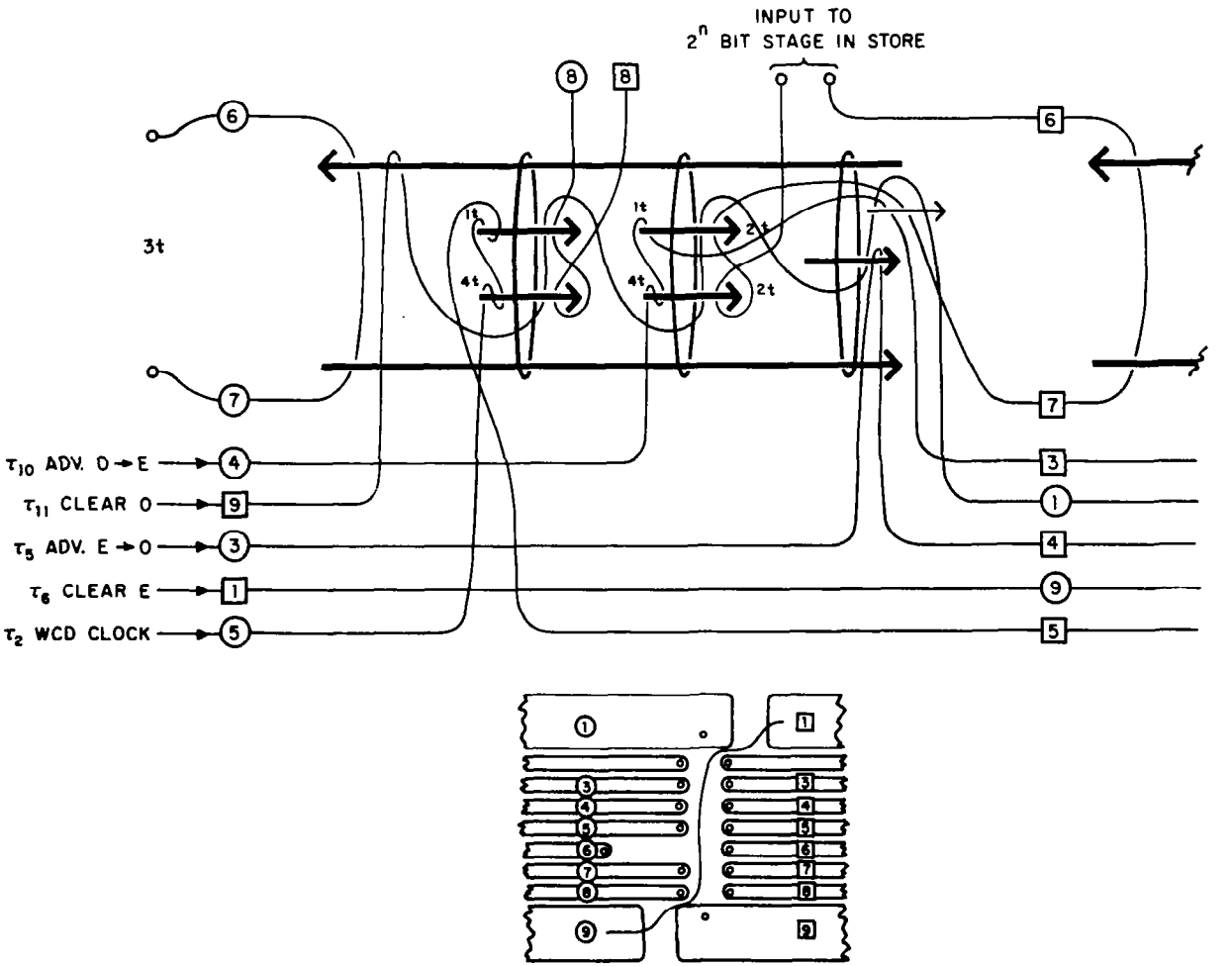


FIG. 13 STOPPER LOGIC CIRCUIT: WEIGHT CURRENT PROGRAMMER

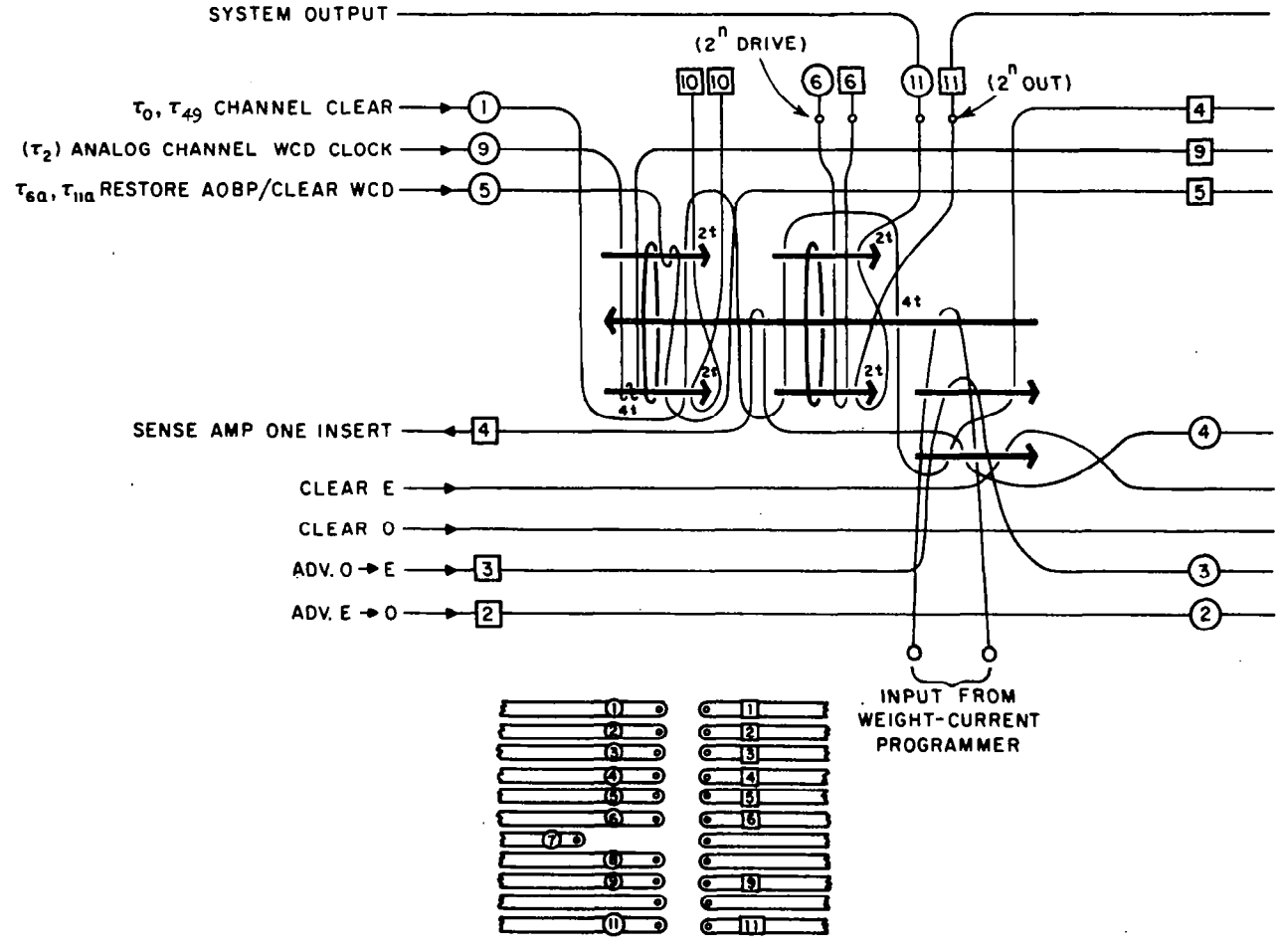


FIG. 14 BUFFER STORE CIRCUIT

that provides the input to one weight current driver. This constitutes an OR circuit. When a logic stage in the programmer has been set to the ONE state, τ_2 will switch the AOBP and therefore switch the flux source core in the driver circuit associated with the stage. When a stage in the buffer store has been set, its AOBP will be switched by (τ_2), which is controlled by the digit channel detector (DCD) circuit, and again the flux source core in the driver associated with this stage is switched. For the analog channels, after a ONE has been stored in a stage of the buffer store, the associated driver is turned on for each comparison by (τ_2). The turn-on from the buffer store is referred to as the repetitive turn-on and that from the programmer as the sequential turn-on. For the digital channels (τ_2) is removed by the DCD circuit and the repetitive turn-on does not occur.

The multipulse driver L_3 - L_4 is the primary pulse power source for the weight-current generator section of the system. A schematic representation of this circuit is given in Fig. 15. There are two principal differences between it and the driver circuit shown in Fig. 6. Driver L_3 - L_4 is turned on at a repetition rate of approximately 50 kc for a short period of time and then it is not turned on again until a delay period of approximately 14 milliseconds has elapsed; this operation is illustrated in Fig. 2. Because of this high repetition rate (for a short time) an RC charging circuit cannot be used in the input circuit, and the transistors are therefore connected directly to the 28-v source.

The second principal difference is the branching circuit in the secondary of T_2. The pulses τ_6 and τ_{6a} begin at the same time but have different amplitudes and different pulse durations. The same is true of τ_{11} and τ_{11a}. The branching circuit effects this pulse relationship. To generate pulse τ_5 (or τ_{10}) energy that is stored in C_1 is transferred into C_6 (or C_{10}); however, simultaneously a portion of this energy is transferred from C_1 into C_{6a} (or C'_{6a}). The transfer into C_6 takes the same length of time to complete as does the transfer into C_{6a}, but C_6 receives the greater energy and serves to provide drive pulse τ_5. The transfer into C_{6a} is not used to provide a drive pulse. The discharge

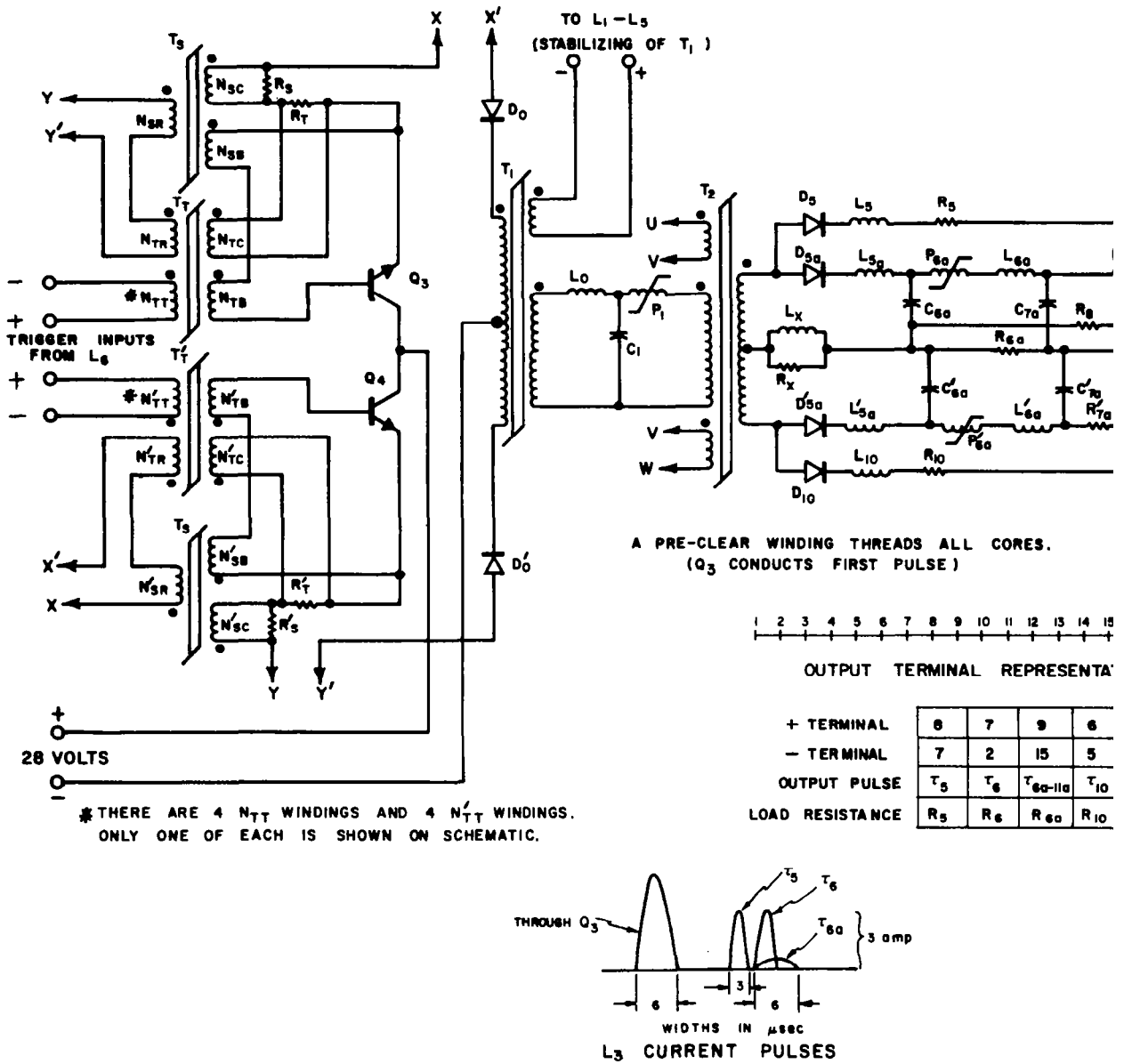


FIG. 15 MULTIPULSE DRIVERS L_3–L_4

of both capacitors (C_{6a} and C_6) begins at the same time, which means that the pulses produced by these discharges, τ_6 and τ_{6a}, begin at the same time. The duration of τ_6 is 3 μsec and the duration of τ_{6a} is 6 μsec. Both pulses τ_{6a} and τ_{11a} go through the common load indicated by R_{6a} on the schematic to reset the AOBP's in the store and to reset the weight current drivers.

Table I summarizes the number of components used in the feasibility breadboard and provides a comparison with the estimate made in Phase I. Appendix A identifies the components and materials used.

Table I

LIST OF COMPONENTS

COMPONENT	ESTIMATED (PHASE I)		REQUIRED (PHASE II)	
MAGNETIC ELEMENTS				
30/50 Memory Cores	--		60	
50/80 Memory Cores	500		360	
300/330 Stopper Toroids	162		95	
Cores for Drivers	--		--	
Pulsactors	40		20	
Square-Loop Transformers	--		26	
Linear Transormers*	--		5	
		702		566
TRANSISTORS				
For Logic Drivers†	10		9	
For Timing Generator Drivers§	16		3	
For Weight-Current Generator Drivers	14		16	
For Sense Amplifier	7		8	
For Oscillator	3		5Δ	
For Interface Amplifiers	--		4	
		50		45
DIODES				
For Drivers	13		23	
For Sense Amplifier	--		6	
For Weight-Current Generator	--		8	
For Interface Amplifiers	--		3	
		13		40
CAPACITORS				
For Drivers	40		38	
For Sense Amplifier	--		12	
		40		50
INDUCTORS FOR DRIVERS		40		26

* 2 for sense amplifier

† $L_1 - L_5$, $L_3 - L_2$

§ $D_1 - D_2$, L_6

Δ Oscillator + D_0

IV SYSTEM EVALUATION AND RECOMMENDATIONS

During the progress of this project, testing of the logic circuits started with a single stage and continued through the progressive increase in the length of logic stages connected to operate as a ring counter. The maximum number of logic circuits so connected in the breadboard is 14 stages. Operating data on the 14-stage ring counter used in the timing generator were obtained including the effect of temperature on margins. These data were obtained initially using the rectangular pulses from laboratory current drivers, and then later the half-sine-shaped pulses of the multipulse driver. The work on the multipulse driver started with circuit tests of the initial, direct-coupled, two-pulse design. Testing progressed through the design of the transformer-coupled multipulse drivers, which provide either four sequential pulses or three pulses that occur in a complex pattern. Experiments have shown that over the temperature range of interest, the multipulse driver output pulses were practically unaltered. A range map of the 14-stage ring counter driven by multipulse drivers D_1 - D_2 is given in Fig. 16. From tests (incomplete) the system power-requirement is estimated to be less than 2-1/2 watts.

The experience gained in building the breadboard model of the feasibility telemetry system has both brought out and aided in identifying areas where future effort will result in an improved system. The first of these areas relates to specific problems which have produced excessive delays or uncertain results during Phase II and for which adequate solutions have not been found to date. The second area relates to additional performance data that are needed for specific circuits. The final area relates to improved system performance obtained by refining those circuits and logic functions where, based on the experience gained to date, the potential for significant improvement exists.

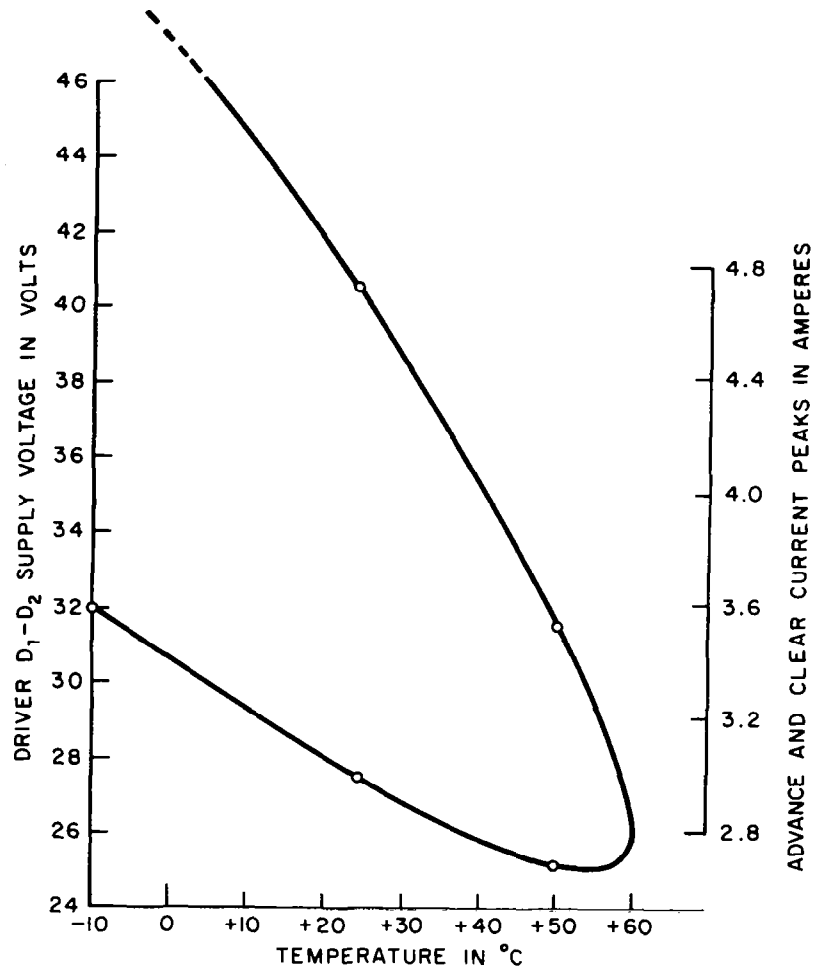


FIG. 16 RANGE MAP FOR 14-STAGE RING COUNTER

The first area pertains to the mechanical assembly used for the logic circuits but also relates to the electrical characteristics of certain portions of the assembly that are determinant for the performance of the logic circuits. The mechanical assembly used in the breadboard was intended to permit (relatively) easy access to the logic circuits to facilitate changes. To achieve this a copper-to-copper pressure contact was used. Obtaining and maintaining a uniformly low resistance in this contact has been a formidable problem. A solder connection, because of the compactness of the assembly and the requirement of heating the assembly to soldering temperature, presents the hazard of the soldering flux and solder flowing into the interior of the assembly, damaging wire insulation and/or producing shorts. The use of HML* insulation eliminates these problems but has produced additional problems of equal or greater magnitude. The method of stripping HML insulation has not been satisfactorily solved. On individual pieces of wire this can be accomplished by several means. However, when stripping is to be done on a circuit assembly containing several wires, and where many assemblies are involved, the methods are not satisfactory. Mechanical stripping has produced abrasion of the insulation and then shorts. Chemical stripping has resulted in excursions wherein insulation was removed from unwanted parts of the wire. Chemical stripping in a controlled manner, which prevents the possibility of excursions, is a much slower and tedious operation. The production of shorts occurred principally where the wires were brought through the copper assembly to the printed circuit strip for interstage connection. This type of damage can cause intermittent and delayed-occurrence shorts. This source of shorts must be eliminated. A mechanical assembly compatible with the low-impedance requirements of the circuits and which does not degrade the inherent high reliability, needs to be designed.

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* Heavy ML, (Pyre-M.L.), T. M. DuPont.

The second area pertains principally to the logic circuits and relates to the effect on the operating range resulting from variations of the basic circuit, particularly those used to achieve the several logic functions. Two findings which occurred in this phase relate to this aspect. A leakage flux problem associated with the stopper cores appeared in the initial Phase II tests of the stopper circuits. This effect had not previously been observed in the circuits tested in Phase I. In these tests different core material was used. The AOBP in the prime channel programmer is not required for this logic function and was removed. This circuit failed to operate and,as an expedient, the AOBP was restored. The reasons for this circuit failure are not fully understood. Additional testing of the basic logic circuits and the interfaces required in this system is needed. This should be directed at determining the quantitative relationships between variation of circuit parameters and circuit performance.

The third area pertains to improvement of the system performance through logic and circuit refinements. This effort would be principally aimed at further reduction in the number of semiconductors and the amount of power required. To accomplish this, further investigations of the multipulse driver circuit, the oscillator and the interfaces between logic circuits and multipulse drivers will be required. It appears probable that as a result of such an effort: the number of transistors and power required per multipulse driver would be reduced; driver L_2 would be realized by a multipulse circuit; the number of transistors required for the oscillator and amplifier circuit would be reduced; the digital channel detection amplifier would be eliminated and the logic for this function simplified; the interface amplifier driven by the 14-stage counter would be eliminated and the length of the 14-stage counter would be reduced to eight stages.

Two other areas can be identified where further reduction in semiconductors may prove possible: the weight-current drivers and the sense amplifiers. The latter may be capable of being realized, at least in part, using all-magnetic circuit techniques.

Appendix A

COMPONENT IDENTIFICATION

Appendix A

COMPONENT IDENTIFICATION

1. LOGIC CIRCUITS (Core identification given in Fig. 8)

Core No.	Manufacturer	Material/Type	Size
1, 2	Indiana General	S-4	330/300/30*
3, 4, 5, 6, 7, 8	Ampex	802-40	50/80/25
9	Electronic Memories Inc.	51-113 B	30/50/15
BMC Pair	Ampex	802-40	50/80/25
BMC Decoupler	Electronic Memories Inc.	51-113 B	30/50/15
Cavity Block Housing	- - -	Copper	
Printed Circuit Board †	G. T. Schjeldahl Co. Teflon x. 4 oz TA Cu	GTA 2127-1	

2. DRIVER CIRCUITS

a. L_1 - L_5 and D_1 - D_2 (See Fig. 6)

T_1: Arnold Engineering
6T5502-H1-AA
Primaries: 20 turns
Secondary: 60 turns
Three strands #28 wire

T_2: Magnetics, Inc.
80525-1/2D MA
Primary: 23 turns
Secondaries: 46 turns } Two strands #26 wire
Stabilizing: U-V, V-W, 1 turn #28 wire

P_1: Arnold Engineering
6T5502-H1-AA
50 turns } Three strands #28 wire

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* Cut ultrasonically from Indiana General Corp. Size 483 S-4 toroids
† For interstage wiring

P_2: P_2': Magnetics Inc.
80598-1/4D MA
90 turns} Two strands #28 wire
Stabilizing: R-P, Q-P, 5 turns #36 wire

P_3': Magnetics Inc.
80598-1/4D MA
77 turns} Two strands #28 wire
Stabilizing: 5 turns #28 wire

P_4': Arnold Engineering
19P 125 73 AA
114 turns #28 wire
Stabilizing: 5 turns #28 wire

T_S: T_S': Indiana General
MC 137
N_{SB}: 33 turns, #30 wire
N_{SC}: 6 turns, #28 wire
N_{SR}: 1 turn, #28 wire

T_T: T_T': Burroughs Corp.
231-002

N_{TB}: 10 turns
N_{TC}: 6 turns
N_{TT}: 2 turns
N_{TR}: 1 turn
} #28 wire

$C_0 = C_0' = 1.5\ \mu f$*
$C_1 = 0.18\ \mu f$
$C_2 = C_2' = 0.056\ \mu f$
$C_3 = 0.056\ \mu f$
$C_3' = 0.082\ \mu f$
$C_4' = 0.106\ \mu f$
$C_5' = 0.09\ \mu f$
} $L_1 - L_5$
$C_3 = C_3' = 0.06\ \mu f$, $D_1 - D_2$

$L_0 = 380\ \mu h$*
$L_1 = L_1' = 15\ \mu h$
$L_2 = 15\ \mu h$

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* All capacitors are polycarbonate type
All chokes wound on ferrite forms equivalent to Indiana General Q1.

$L_2' = 8\ \mu h$
$L_3' = 11\ \mu h$ } $L_1 - L_5$

$L_2' = 15\ \mu h$, $D_1 - D_2$

$R_s = R_s' = 1\ \Omega$
$R_T = R_T' = 6.8\ \Omega$
$R_b = R_b' = 270\ \Omega$
$R_1 = R_1' = 3.3\ \Omega$
$R_2 = R_2' = 5.6\ \Omega$
$R_3 = 27\ \Omega$

$R_1'' = 0.5\ \Omega$
$R_2'' = 0.5\ \Omega$
$R_3' = R_4' = 1\ \Omega$ } $L_1 - L_5$
$R_5' = 15\ \Omega$

$R_1'' = R_2'' = 0$
$R_5' = 27\ \Omega$ } $D_1 - D_2$

b. $L_3 - L_4$ (see Fig. 15)

T_s: T_s': Indiana General
MC 137
N_{SB}: 11 turns N_{SC}: 5 turns
N_{SR}: 1 turn
All windings #30 wire

T_T: T_S': Burroughs Corp. 231-002
N_{TB}: 8 turns N_{TC}: 5 turns
N_{TR}: 1 turn
N_{TT} consists of 4 separate windings,
2 with one turn each, and 2 with two turns.
All windings #30 wire

T_1: Magnetics Inc.
80525-1/2D MA
Primaries: 57 turns } #28 wire
Secondary: 120 turns }
Stabilizing: 1 turn, #26 wires

T_2: Magnetics Inc.
80525 1/4D MA
Primary } 40 turns, two
Secondaries } strands #28 Wire
U-V = V-W = 1
Alternate: 80618-1/4 MA
3 windings of 35 turns each

P_1: Magnetics Inc.
80525 1/2 D MA
64 turns, 3 strands of #26 wire

P_6: P_{11}: Arnold Engineering
19 P 125 73 AA
112 turns #28 wire

P_{6a}: P'_{6a}: Arnold Engineering
19P 125 73 AA
122 turns #28

$L_0 = 16\ \mu h$

$L_5 = L_{10} = 4\ \mu h$

$L_{5a} = L'_{5a} = 18\ \mu h$

$L_{6a} = L'_{6a} = 180\ \mu h$

$R_s = R'_s = 1.3\ \Omega$

$R_t = R'_t = 4.7\ \Omega$

$R_8 + R_5 = R_{10} + R_8 = 1.3\ \Omega$
$R_9 + R_6 = R_{11} + R_9 = 3.3\ \Omega$
} See Note

$R_{6a} = 4.7\ \Omega$

$R_{7a} = R'_{7a} = 110\ \Omega$

$R_7 = R_{12} = 22\ \Omega$

$C_1 = 0.12\ \mu f$

$C_6 = C_{10} = 0.13\ \mu f$

$C_7 = C_{12} = 0.22\ \mu f$

$C_{6a} = C_{6a} = 0.037\ \mu f$

$C_{7a} = C'_{7a} = 0.03\ \mu f$

Diodes: IN697

Transistors: 2N2890

Note: $R_8 + R_5 = R_{10} + R_5 \cong R_8 = R_{10}$
$R_9 + R_6 = R_9 + R_{11} \cong R_6 = R_{11}$

c. L 6 (See Fig. 7)

P_{2-6}: Magnetics Inc.
80618 1/4 DMA
108 turns #28 wire
(Except #26 used on P_2)

P_{7-8}: Magnetics Inc.
80618 1/2 DMA
68 turns #26 wire

T_S: Burroughs Corporation
231-002
N_B: 24t N_C: 6t
N_R: 8t N_T: 1t
All windings #28 wire

D_1: IN697

Q_6: 2N2890

$C_0 = 0.27\ \mu f$
$C_1 = 0.09\ \mu f$
$C_2 = 0.12\ \mu f$
$C_3 = 0.12\ \mu f$
$C_4 = 0.12\ \mu f$
$C_5 = 0.12\ \mu f$
$C_6 = 0.12\ \mu f$
$C_7 = 0.14\ \mu f$
$C_8 = 0.12\ \mu f$

$R_{1T} = 680\ \Omega$
$R_{8T} = 1K\ \Omega$
$R_b = 330\ \Omega$
$R_c = 27\ \Omega$

$L_1 = 18\ \mu h$
$L_2 = 15\ \mu h$
$L_3 = 15\ \mu h$
$L_4 = 8\ \mu h$
$L_5 = 7\ \mu h$
$L_7 = 4\ \mu h$

NASA-Langley, 1966 CR-621